(19)日本国特許庁（JP）　(12)公開特許公報（A）　(11)特許出願公開番号

特開平11－150248

(43)公開日　平成11年(1999)6月2日

| (51)Int.Cl.* | 識別記号 | FI | |
|---|---|---|---|
| H01L 27/108 | | H01L 27/10 | 681F |
| 21/8242 | | | 621C |
| | | | 621B |

審査請求 有　請求項の数9　FD　（全 6 頁）

(21)出願番号　特願平9－331211

(22)出願日　平成9年(1997)11月14日

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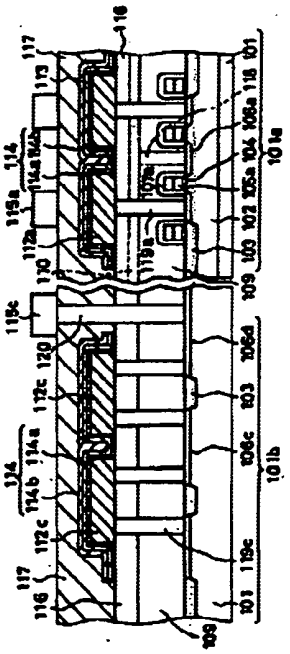
(54)【発明の名称】　半導体記憶装置

(57)【要約】

【課題】ＤＲＡＭの周辺回路領域に存在する抵抗素子の占有面積を縮小する半導体記憶装置の提供。

【解決手段】シリコン基板の表面に形成された拡散層と層間絶縁膜中に形成されたスタック型キャパシタの下部電極を接続用の部材として、特に高抵抗が得られる、スタック型キャパシタの下部電極と拡散層をつなぐ（多結晶シリコンを埋め込んだ）コンタクトを接続し、これらすべてを直列に配列した構造からなる抵抗素子を設けている。これにより、平面的な占有面積に対する抵抗値を増大することが可能となり、抵抗素子の占有面積を縮小する事が容易になる。



# PATENT ABSTRACTS OF JAPAN

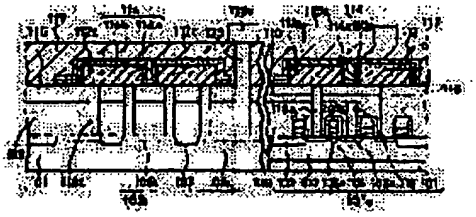
(11)Publication number : 11-150248
(43)Date of publication of application : 02.06.1999

(51)Int.Cl. H01L 27/108
H01L 21/8242

(21)Application number : 09-331211 (71)Applicant : NEC CORP
(22)Date of filing : 14.11.1997 (72)Inventor : SAKAO MASATO

## (54) SEMICONDUCTOR MEMORY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To reduce an occupying area of a resistor element by performing connection to a neighboring diffused layer via an electrode for the resistor element and a contact for the resistor element, sequentially connecting contacts for a plurality of the resistor elements through an electrode for the resistor element and a diffusing layer, and constituting the resistor element.
SOLUTION: At the same time of formation of a capacitor contact hole 119a of a memory cell region 101a and a storage electrode 112a, a contact hole (RC) 119c for a resistor element and a resistor-element electrode (electrode) 112c are formed on an n+-type source/drain region 106 of a peripheral circuit region 101b, so as to be connected to the neighboring region. The resistor element is formed by connecting the region 106c, the capacitor contact hole 119a and the electrode 112c for the resistor element. An aluminum wiring electrode 115c is connected to a drawing region 106d via a contact hole 120 and further connected to the electrode 112c via the drawing region 106d and the RC 119c. The connection is performed from the electrode 112c via the RC 119c to the neighboring region 106c.



LEGAL STATUS

| | |
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| [Date of request for examination] | 14.11.1997 |
| [Date of sending the examiner's decision of rejection] | |
| [Kind of final disposal of application other than the examiner's decision of rejection or application converted registration] | |
| [Date of final disposal for application] | |
| [Patent numb r] | 3039495 |
| [Date of registration] | 03.03.2000 |
| [Number of appeal against xamin r's d cision of rejection] | |

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[Claim(s)]

[Claim 1] The semiconductor device characterized by to have had the contact for resistance elements for connecting the electrode for resistance elements on the diffusion layer on the front face of a substrate, and the insulating layer prepared on the aforementioned substrate, to have connected with the next aforementioned diffusion layer through another contact for resistance elements linked to the aforementioned electrode for resistance elements and the aforementioned electrode for resistance elements which extend even in the position on the next diffusion layer, to have connected two or more contacts for resistance elements with the electrode for resistance elements one after another through a diffusion layer, and to constitute a resistance element.

[Claim 2] The semiconductor device according to claim 2 characterized by what the resistance element of the aforementioned circumference circuit section of the semiconductor device with which the aforementioned resistance element was equipped with the memory cell array equipped with two or more memory cells of stack type capacitor structure and the circumference circuit section is constituted, the aforementioned contact for resistance elements consists of the same material as capacity contact of the aforementioned stack type capacitor, and the aforementioned electrode for resistance elements consists of the same material as a part of electrode of the aforementioned stack type capacitor.

[Claim 3] The semiconductor device according to claim 2 characterized by using the pad layer for contact cash drawers formed in the interval section of the word line of the memory cell section equipped with the aforementioned stack type capacitor as a conductor film for resistance elements of the aforementioned circumference circuit section.

[Claim 4] The semiconductor device according to claim 1 characterized by having had the contact for cash draw rs which connects a wiring layer and the diffusion layer for cash drawers on the aforementioned front face of a substrate, and considering the aforementioned diffusion layer for cash drawers, and the aforementioned electrode for

resistance elements as the composition connected by the af rementioned contact for resistance elements.

[Claim 5] the aforementioned contact for resistance elements ·· connection of the aforementioned insulator layer ·· a semiconductor device given in any 1 of claim 1 **** 4 which embed polycrystal silicon at a hole, are formed and are characterized by the bird clapper

[Claim 6] The semiconductor memory characterized by what a part of accumulation electrode in the memory cell equipped with the stack type capacitor and capacity contact are used as the electrode for resistance elements in the circumference circuit section, and resistance element contact, and the high resistance element of the aforementioned circumference circuit section is formed for by connecting through a diffusion layer.

[Claim 7] The semiconductor memory characterized by having the resistance element which consists of structure which connected the contact which connects the lower electrode of the aforementioned stack type capacitor, and the diffusion layer of a memory cell transistor as a member for connection between the diffusion layer formed in the front face of a semiconductor substrate, and the lower electrode of the stack type capacitor formed into the layer insulation film, and arranged these in series.

[Claim 8] Stack type capacitor. The accumulation electrode which constitutes this. The cell array section which consists of an array of the memory cell containing the contact portion which connects the diffusion layer for memory cells, and the aforementioned accumulation electrode and the aforementioned diffusion layer for memory cells, and the circumference circuit section which contains a resistance element at least. It is the semiconductor memory equipped with the above, and the aforementioned resistance element carries out the series connection of the contact for resistance elements which connects the electrode for resistance which consists of same members as the contact portion which connects the aforementioned accumulation electrode, the aforementioned diffusion layer for memory cells, and the aforementioned accumulation electrode and the aforementioned diffusion layer for memory cells, a diffusion layer, and the aforementioned resistance electrode and the aforementioned diffusion layer, and is characterized by the bird clapper.

[Claim 9] The semiconductor memory according to claim 1 to which the aforementioned electrode for resistance is characterized by consisting of same members as a part of aforementioned accumulation electrode.

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention relates to the semiconductor device which contains (DRAM) in dynamic random access memory about a semiconductor memory.

[0002]

[Description of the Prior Art] In the semiconductor device containing an MOS transistor, when a voltage stabilizer including a feedback function like for example, voltage detection or an AD(analog-to-digital)-DA (digital analog) conversion circuit is contained, a resistance element is needed for the circuit which constitutes this semiconductor device.

[0003] It is desirable that high resistance is required for these resistance elements in order to reduce change of the current by the current which flows a resistance element, and there are few errors of the resistance for which it depends on the fluctuation of a manufacturing process (variation) further, for example, the resistance which is 1 M omega - about 10 M omega is demanded.

[0004] the 0.2um(s) (micrometer) design rule grade demanded these days is detailed -- with the semiconductor device containing the MOS transistor which turned, the conductor film used for a wiring material is in the inclination of the reduction in resistance, a gate electrode consists of metal polycide films a metal silicide film comes to carry out a laminating to N+ type polycrystal silicon film, and other lower layer wiring tends to consist of metal silicide films

[0005] For example, also in the semiconductor device containing DRAM which has the memory cell of a stack type capacitor, although the main purpose differs from low resistance-ization with adoption of refractory metals, such as a tantalum oxide (Ta 2O5) film, it is in the inclination transposed to the cascade screen of a titanium-nitride (TiN) film and a tungsten silicide (WSi) film, for example from the component N+ type polycrystal silicon film of the cell plate electrode of a memory cell.

[0006] Generally as a component of the above-mentioned resistance element, 2nd N+ type polycrystal silicon film separately prepared on the front face of a field insulator layer is desirable. In order to reduce relatively the error of the resistance for which it depends on fluctuation of a manufacturing process though semiconductor devices, such as an MOS transistor, are formed by 0.2um design rule in this case, the resistance element is formed with the line breadth of about 0.8 ums.

[0007]

[Problem(s) to be Solved by the Invention] In the above-mentioned common semiconductor device or the semiconductor device containing DRAM, it has the trouble that the occupancy area of a resistance element becomes a remarkable size. For

example, when resistance forms the resistance element which is 5 M omega with N+ type polycrystal silicon film (the 2nd) whose layer resistance is 50ohms / ** grade in about 150nm of thickness, this occupancy area is as follows. For example, if it has the gestalt which has the interval of 0.8um(s) and moved in a zigzag direction, an occupancy area required for this resistance element will be set to about two 128x103um.

[0008] Therefore, this invention is made in view of the above-mentioned trouble, and the purpose is in offering the semiconductor device which reduces the occupancy area of a resistance element, maintaining relative reduction of the error of the resistance of the resistance-element separation which carries out body dependence at fluctuation of a manufacturing process for achievement of detailed-izing of a semiconductor device.

[0009]

[Means for Solving the Problem] In order to attain the aforementioned purpose, the semiconductor device of this invention is characterized by to have had the contact for resistance elements for connecting the electrode for resistance elements on the diffusion layer on the front face of a substrate, and the insulating layer prepared on the aforementioned substrate, to have connected with the next diffusion layer through the aforementioned electrode for resistance elements, and another contact for resistance elements, to have connected two or more contacts for resistance elements with the aforementioned electrode for resistance elements one after another through the diffusion layer, and to constitute a resistance element.

[0010] In this invention, it consists of a resistance element of the aforementioned circumference circuit section of the semiconductor device with which the aforementioned resistance element was equipped with the memory cell array equipped with two or more memory cells of stack type capacitor structure, and the circumference circuit section, and the aforementioned contact for resistance elements is characterized by what the aforementioned electrode for resistance elements consists of the same material as the lower electrode of the aforementioned stack type capacitor in the same members as capacity contact of the aforementioned stack type capacitor.

[0011] In this invention, the pad layer for contact cash drawers formed in the interval section of the word line of the memory cell section equipped with the aforementioned stack type capacitor is used as a conductor film for resistance elements of the aforementioned circumference circuit section.

[0012]

[Embodiments of the Invention] The gestalt of operation of this invention is explained. this invention is set in the gestalt of the desirable operation. The diffusion layer on the front fac of a substrate (106c of the cross section of drawing 1 , and the plan of drawing

3 ), It has the contact for resistance elements (119c of drawing 1 and drawing 3 ) for connecting the electrode for resistance elements on the layer insulation film prepared on the substrate (112c of drawing 1 and drawing 3 ). It connects with the next diffusion layer through another contact for resistance elements linked to the electrode for resistance elements which extends even in the position on the next diffusion layer, and this electrode for resistance elements (119c of drawing 1 ). Wiring (115c of drawing 1 and drawing 3 ), the contact for drawers (120 of drawing 1 and drawing 3 ), Two or more above-mentioned contacts for resistance elements (119c of drawing 1 and drawing 3 ) are connected with the electrode for resistance elements (112c of drawing 1 and drawing 3 ) one after another through a diffusion layer (106c of drawing 1 and drawing 3 ), and the resistance element of desired resistance consists of diffusion layers for drawers (106d of drawing 1 and drawing 3 ). This is enabled to increase the resistance to a superficial occupancy area, and it becomes easy to reduce the occupancy area of a resistance element.

[0013] In the gestalt of operation of this invention, it consists of a resistance element of the aforementioned circumference circuit section of the semiconductor device with which the aforementioned resistance element was equipped with the memory cell array equipped with two or more memory cells of stack type capacitor structure, and the circumference circuit section, the contact for resistance elements consists of the same material as capacity contact of the aforementioned stack type capacitor, and the electrode for resistance elements (112c of drawing 1 ) consists of the same material as the lower electrode (112a of drawing 1 ) of the aforementioned stack type

[0014] In the gestalt of operation of this invention, a desired resistance element can be formed by using the pad layer for contact cash drawers formed in the interval section of the word line of the memory cell section as a conductor film for resistance elements of the circumference circuit section, turning formation of a memory cell easily.

[0015] Moreover, it becomes possible to form resistance element sufficient in small area by attaching the upper surface and the side of a conductive layer of a conductive layer and this layer which constitute a word line for the conductor film for the resistance elements of the circumference circuit section so that a wrap insulator layer front face may be met.

[0016]

[Example] Next, the example of this invention is explained with reference to a drawing. Drawing 1 is a cross section for explaining the semiconductor memory of the 1st example of this invention, and shows the memory cell field and circumference circuit field of a semiconductor memory.

[0017] As for the memory cell field of a semiconductor memory, and 101b, in drawing 1, 101a is [ the conductivity type of a circumference circuit field and 101 ] a p type silicide substrate.

[0018] The P well 102 is formed in field 101a in which a memory cell array etc. is formed, and the field oxide film 103 is formed in the isolation field of the front face of the P type silicon substrate 101 including the front face of the P well 102.

[0019] N well and P well (not shown) are formed in circumference circuit field 101b. In addition, it is formed in circumference circuit field 101b, and N well with the depth of junction deeper (it is another) than a **** well may be beforehand formed in memory cell field 101a. Moreover, an N type silicon substrate may be adopted instead of the P type silicon substrate 101.

[0020] Gate electrode 105a which serves as a word line through the gate oxide film 104 is formed in memory cell field 101a. This gate electrode consists of a polycide which consists of laminated structures of WSi or TiSi, and polycrystal silicon.

[0021] The gate electrode which is not illustrated [ of the same composition as this gate electrode 105a ] is formed also in circumference circuit field 101b.

[0022] The cell transistor which constitutes a memory cell consists of gate electrode 105a and n- type source drain field 106a.

[0023] n+ type source drain field 106c of circumference circuit field 101b constitutes the transistor (not shown) of a circumference circuit field.

[0024] Gate electrode 105a is covered with oxide-film 107a in the upper surface and side, respectively. it connects with n- type source drain field 106a at a memory cell -- as -- bit line contact -- a hole 118 and capacity contact -- a hole -- 119a is formed

[0025] bit line contact -- a bit line 110 is connected to a hole 118 this bit line contact -- a hole 118 and capacity contact -- polycrystal silicon is embedded at hole 119a

[0026] capacity contact -- accumulation electrode 112a is connected to hole 119a, and a cell capacitor is formed in it with the capacity insulator layer 113 and the cell plate 114

[0027] The cell plate 114 consists of a laminated structure of WSi film 114a and TiN film 114b. These structures are isolated between the 1st layer by the insulator layer 109, the insulator layer 116 between the 2nd layer, and the insulator layer 117 between the 3rd layer. Moreover, aluminum wiring 115of memory cell field 101a a becomes a component for choosing a word line.

[0028] capacity contact of these memory cell sections -- a hole -- the formation [ of 119a and accumulation electrode 112a ], simultaneously n+ type source drain field 106c top of circumference circuit field 10b -- the contact for resistance elements -- a hole -- 119c and electrode 112c for resistance elements form so that adjoining n+ type source drain field

may be connected in series

[0029] That is, accumulation electrode 112a and electrode 112c for resistance elements are the same material, and it is formed at the same process.

[0030] moreover, capacity contact ·· a hole ·· 119a and the contact for resistance elements ·· a hole ·· 119c and embedded polycrystal silicon are formed at the same process by the same material

[0031] thus, a resistance element ·· n+ type source drain field 106c and capacity contact ·· a hole ·· 119c and electrode 112c for resistance elements are connected, and it is constituted

[0032] 106d of n+ type source drain fields for cash drawers and contact for connecting a resistance element with external wiring at drawing 1 ·· a hole 120 and aluminum wiring 115c are shown

[0033] These connection relations are explained with reference to the plan of the resistance-element section shown in drawing 3 . In addition, circumference circuit field 101b of drawing 1 is the cross section of the direction of an A-A line in drawing 3 .

[0034] It connects through a hole 120. from aluminum wiring 115c ·· pulling out ·· business ·· 106d of n+ type source drain fields ·· contact ·· 119c is minded. 106d of n+ type source drain fields for cash drawers ·· leading ·· the contact for resistance elements ·· a hole ·· 119c ·· minding ·· electrode 112c for resistance elements ·· connecting ·· moreover, the contact for resistance elements from this electrode 112for resistance elements c ·· a hole ·· the contact for resistance elements which has a high resistance field by connecting with the next n+ type source drain field 106c ·· a hole ·· incorporating 119c to a resistance element continuously ·· a facet ·· resistance [ **** ] is securable by the product

[0035] According to the first example of this invention, the not use of a superficial resistive layer but height direction in a device (perpendicular direction) like before can also be used as a resistance element, and has the operation effect of securing the length of an efficiency-resistance element.

[0036] For example, if it forms by 0.2um design rule, the direction formed in the array (size relation) as the memory cell field formed simultaneously with the same array of n+ type source drain field 106c can reduce relatively the error of the resistance depending on fluctuation of a manufacturing process, and can also reduce occupancy area.

[0037] About reduction of the occupancy area of the resistance element which is the main purpose of this invention, this example does the following operation effects so.

[0038] The longitudinal direction of n+ type source drain field 106c serves as [ an interval with 0.2um(s) and the contiguity section ] 0.8um(s), and width f face serves as

0.2um(s). Resistance of the contact for resistance elements is about 1kohm, and since layer resistance of n+ type source drain field 106c is 100ohm/**, as for the occupancy area of a 5-M omega resistance element, layer resistance of 150ohm/**, and the electrode for resistance elements is set to about two 40x21um by it.

[0039] Drawing 2 is a cross section for explaining the semiconductor memory by the second example of this invention.

[0040] In drawing 2, the same reference mark is given to the element the same as that of drawing 1, or equivalent. When drawing 2 is referred to, the difference between the second example of this invention and the first example shown in drawing 1 is a point that accumulation electrode 112a of the first example of the above is constituted from the second example by being replaced with 112f of cylindrical accumulation electrodes, and the structure with which 112g of electrodes for resistance elements constitutes 112d of plinths of the 112f of the aforementioned cylindrical accumulation electrodes.

[0041] Since layer resistance of the electrode for resistance elements explained in the first example of the above serves as 400ohms / ** grade according to this second example, the occupancy area of a resistance element becomes reducible from the first example of the above further, for example, is set to about two 40x11um.

[0042] furthermore, the contact for resistance elements -- since especially the resistance of the contact for resistance elements is changed by the concentration of polycrystal silicon and the heat treatment temperature which joins this embedded at the hole, it can constitute a resistance element from occupancy area [ **** ] also to reduction of the element in chip level further with it

[0043]

[Effect of the Invention] As explained above, according to this invention, the effect which is the occupancy area of a resistance element of being reducible is done so.

[0044] The reason is as follows. Contact embedding the polycrystal silicon which connects the diffusion layer formed on the surface of the silicon substrate in this invention, the lower electrode of the stack type capacitor with which especially high resistance is obtained considering the lower electrode of the stack type capacitor formed into the layer insulation film as a member for connection, and a diffusion layer was connected, and the resistance element which consists of structure which arranged these [ all ] in series is prepared. This is enabled to increase the resistance to a superficial occupancy area, and it becomes easy to reduce the occupancy area of a resistance element.

[Brief Description of the Drawings]

[Drawing 1] It is the cross section showing the composition of the first example of this

invention.

[Drawing 2] It is the cross section showing the composition of the second example of this invention.

[Drawing 3] It is the plan showing the composition of the first example of this invention.

[Description of Notations]

101a Circumference circuit field

101b Memory cell field

101 Silicon Substrate

102 P Well

103 Field Oxide Film

104 Gate Oxide Film

105a Gate electrode

106a n- type source drain field

106c n+ type source drain field

106d n+ type source drain field for cash drawers

107a Oxide film

109 Insulator Layer between 1st Layer

110 Bit Line

112a Accumulation electrode

113 Capacity Insulator Layer

114 Cell Plate

114a Titanium-nitride film

114b Tungsten silicide film

115a, 115c Aluminum wiring

116 Insulator Layer between 2nd Layer

117 Insulator Layer between 3rd Layer

118 Bit Line Contact -- Hole

119a capacity contact -- a hole

120 Contact -- Hole

【００４３】

【発明の効果】以上説明したように、本発明によれば、抵抗素子の占有面積の縮小することができる、という効果を奏する。

【００４４】その理由は次の通りである。本発明においては、シリコン基板の表面に形成された拡散層と層間絶縁膜中に形成されたスタック型キャパシタの下部電極を接続用の部材として、特に高抵抗が得られる、スタック型キャパシタの下部電極と拡散層をつなぐ、多結晶シリコンを埋め込んだコンタクトを接続し、これらすべてを直列に配列した構造からなる抵抗素子を設けている。これにより、平面的な占有面積に対する抵抗値を増大することが可能となり、抵抗素子の占有面積を縮小する事が容易になる。

【図面の簡単な説明】

【図１】本発明の第一の実施例の構成を示す断面図である。

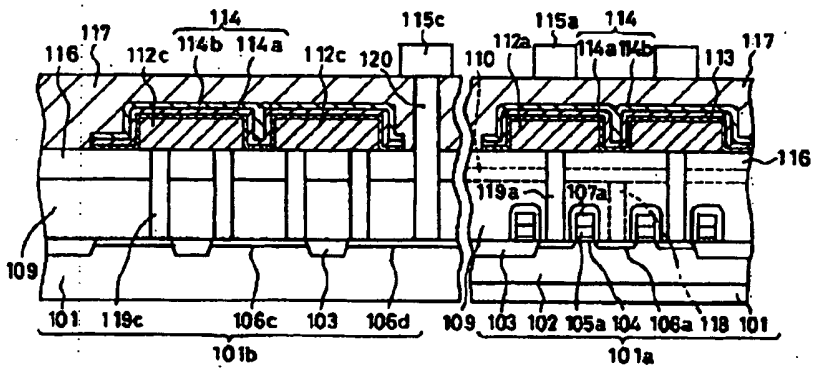
【図２】本発明の第二の実施例の構成を示す断面図である。

【図３】本発明の第一の実施例の構成を示す平面図である。

【符号の説明】

１０１ａ　周辺回路領域
１０１ｂ　メモリセル領域
１０１　シリコン基板
１０２　Ｐウェル
１０３　フィールド酸化膜
１０４　ゲート酸化膜
１０５ａ　ゲート電極
１０６ａ　ｎ－型ソース・ドレイン領域
１０６ｃ　ｎ＋型ソース・ドレイン領域
１０６ｄ　引出し用ｎ＋型ソース・ドレイン領域
１０７ａ　酸化膜
１０９　第１層間絶縁膜
１１０　ビット線
１１２ａ　蓄積電極
１１３　容量絶縁膜
１１４　セルプレート
１１４ａ　窒化チタン膜
１１４ｂ　タングステンシリサイド膜
１１５ａ，１１５ｃ　アルミ配線
１１６　第２層間絶縁膜
１１７　第３層間絶縁膜
１１８　ビット線コンタクト孔
１１９ａ　容量コンタクト孔
１２０　コンタクト孔

【図１】



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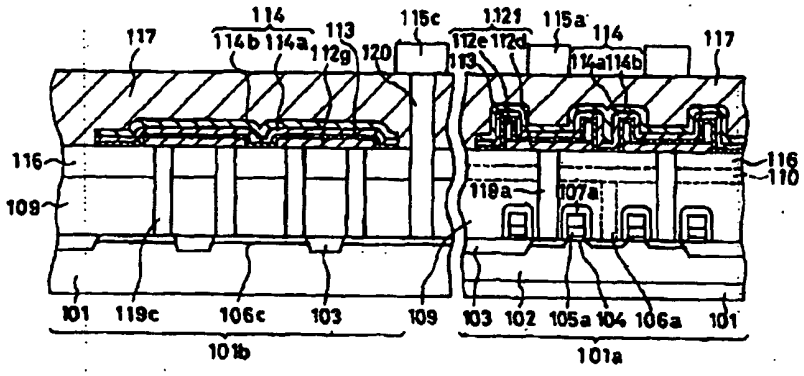
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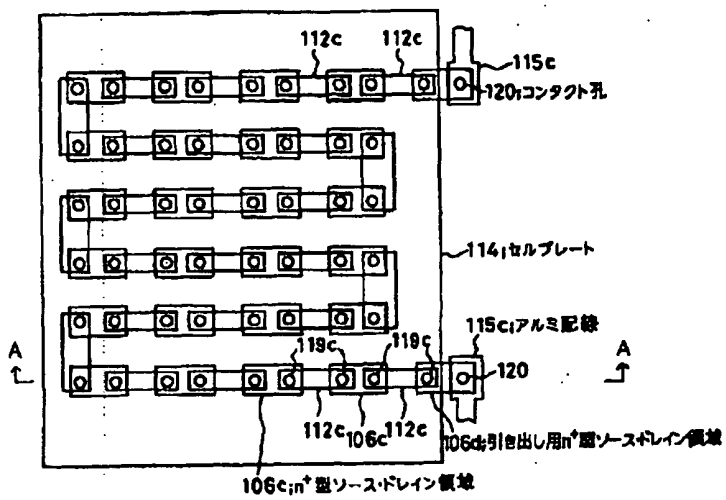
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